REMARKS

The Examiner's withdrawal of the objections to the claims, the title, and the drawings in the "DETAILED ACTION" is noted with appreciation. It is acknowledged that any enablement and indefiniteness rejections were also indicated in the current Office Action to have been overcome by the previous Reply.

However, it is noted that on the "Office Action Summary" form at item "10)", it appears that the box indicating that the Examiner objects to the drawings has inadvertently remained marked. If this is an oversight, it is respectfully requested that the objection box be unmarked and that the approval box be marked in the next communication from the Office. Otherwise, it is respectfully requested that a clarification be provided.

Claims 1-73 are presently pending in the instant Application. Although no claims are canceled, amended, or added by this Reply, the pending claims are reproduced above in final form for the convenience of the Office.

With the current and final Office Action, claims 33-42, 47, and 54 were allowed. Claims 1-32, 43-46, 48-53, and 55-73 were rejected "under 35 U.S.C. 103(a) as being unpatentable over Manning (USPN 6,288,954) in view of Kajigaya et al. (USPN 5,426,616)."

Of the pending claims 1-73, claims 1, 17, 33, 43, 47, 53, 54, 60, and 63 are independent.

Of these independent claims, claims 33, 47, and 54 are allowed.

The allowability of the six other independent claims 1, 17, 43, 53, 60, and 63 is addressed further below.

Although each pending dependent claim includes additional element(s) militating toward allowability, it is respectfully submitted that the dependent claims are allowable at least for the reasons given below in connection with their respective independent claim 1, 17, 43, 53, 60, or 63.

It is respectfully requested that the following arguments be entered and considered by the Examiner.

I. The rejection of claims 1, 17, 43, 53, 60, and 63 under 35 U.S.C. 103(a) cannot be sustained under the facts or the law.

A. There is insufficient motivation to combine Manning and Kajigaya et al.

The current Office Action reads at the last two full sentences on page 2, "However, Manning does not expressly disclose the details for the circuit to generate a reference voltage Vref. Kajigaya et al. disclose, in Figs. 27 and 37, a specific circuit to generate a reference voltage providing variable gain with high accuracy." In contradistinction to the former of the two above-quoted sentences, Fig. 3 of Manning "is a schematic diagram of an embodiment of the reference-signal generator of FIG. 2." (Manning, column 2, lines 57-58.) At column 3, lines 3-5, Manning reads, "... on-board reference-signal generator 32, which in one embodiment is used to internally generate a reference signal Vrefint during testing of the circuit."

The disclosure and/or teachings of Manning, particularly with regard to Fig. 3 and the text related thereto, appear to vitiate the obviousness motivation as provided by the Office Action at the first full sentence on page 3, which reads "Therefore, it would have been obvious for one skilled in the art to use the specific circuit to generate a reference voltage of Kajigaya et al. for the broad circuit to generate a reference voltage of Manning for the expected results of variable gain with high accuracy."

In summary, Manning includes disclosure (e.g., textual description and drawings) of details for a reference voltage generator. The reference voltage

generator of Manning is simpler and cheaper to implement, and the voltage generating details of Kajigaya et al. require a greater chip surface area and are more complex and consequently more costly. Thus, it is respectfully submitted that there was insufficient motivation at the time of the invention to look to Kajigaya et al. for details of a reference voltage generator when Manning provided such details; thus, there was insufficient motivation to combine Manning and Kajigaya et al.

B. Even assuming, *arguendo*, that Manning and Kajigaya et al. could have been combined for some purpose, any such combination would not have resulted in the claimed invention.

1. Any combination of Manning and Kajigaya et al. would have resulted in the reference-signal generator 32 of Manning being replaced by the reference voltage generator (VRG) of Kajigaya et al., not the standard voltage generator (VLG) as applied in the Office Action.

The current Office Action reads at the last two full sentences on page 2, "However, Manning does not expressly disclose the details for the circuit to generate a reference voltage Vref. Kajigaya et al. disclose, in Figs. 27 and 37, a specific circuit to generate a reference voltage providing variable gain with high accuracy." In contradistinction to the latter of the two above-quoted sentences, Fig. 27 is directed to a "STANDARD VOLTAGE GENERATOR (VLG)", and Fig. 37 is directed to a "FUSE CIRCUIT (FC)". (See, Kajigaya et al., Figs. 27 and 37, in conjunction with the overall view provided by Fig. 35.) Furthermore, Kajigaya et al.

separately describes what it terms a reference voltage generator ("REFERENCE VOLTAGE GENERATOR (VRG)", Figs. 32 and 35 of Kajigaya et al.).

The components of Kajigaya et al. that are applied against the claims by the Office Action are part of the standard voltage generator (VLG) thereof and not part of the reference voltage generator (VRG) thereof. Hence, the components of Kajigaya et al. that are asserted to correspond to claim elements are part of the standard voltage generator (VLG) thereof and not part of the reference voltage generator (VRG) of Kajigaya et al. Also, it is respectfully submitted that no components of the reference voltage generator (VRG) (Fig. 32) of Kajigaya et al. correspond to elements of the invention as claimed.

In other words, even assuming, *arguendo*, that one of ordinary skill in the art would have combined Manning and Kajigaya et al., one of ordinary skill in the art would have substituted the reference voltage generator (VRG) of Kajigaya et al in place of the reference-signal generator 32 of Manning. As noted above, the reference voltage generator (VRG) of Kajigaya et al. does not have components corresponding to the claimed elements. Thus, it is respectfully submitted that a combination of Manning and Kajigaya et al. would not have resulted in the claimed invention.

2. Any combination of Manning and Kajigaya et al. in a manner as set forth in the Office Action (which appears to supplant the reference-signal generator 32 of Manning with the standard voltage generator (VLG) of Kajigaya et al.) necessarily creates a hypothetical situation that cannot render the claims obvious.

By way of example, claim 1 reads in full:

> 1. An integrated circuit, comprising:
>
> one or more components, including a feedback component, that receive a distributed voltage, wherein the feedback component of the one or more components has substantially similar input characteristics to at least one other component of the one or more components; and
>
> a voltage driver that produces a compensated voltage;
>
> wherein the compensated voltage is distributed to form the distributed voltage at the one or more components, and the distributed voltage is degraded relative to the compensated voltage; and
>
> wherein the voltage driver is responsive to feedback from the feedback component as derived from the distributed voltage to adjust the compensated voltage so that the distributed voltage is approximately equal to a nominal voltage.

The Office Action reads in its rejection of claim 1 at the last paragraph starting at the bottom of page 2 and continuing onto page 3, "This to generate a reference voltage is seen to include 'a feedback receiver Q9-Q10, R10-R18 and Q58-Q65, Q49, R1-R9 and Q41-Q48 or Q3)', 'a reference voltage driver (OA1, OA2 or Q1-Q2 and Q50-Q52)', 'a register (DEC1 and DEC2)' and a counter (CTRN and CTRB)'."

Assuming, *arguendo*, that the above correspondences as set forth in the Office Action comport with 35 U.S.C. §§ 102 and 103, the 'feedback component/receiver' of Q9-Q10, R10-R18, and Q58-Q65 receives an output from the 'reference voltage driver' of OA1. This output of the 'reference voltage driver' is the voltage between Q7 and Q55 (of op amp OA1 as shown in the standard voltage generator (VLG) of Fig. 27 of Kajigaya et al.) and is provided to the 'feedback component/receiver' at Q9.

For this combination and these correspondences to render claim 1 obvious, this output voltage must correspond to the **compensated voltage** produced by the **voltage driver** as recited in claim 1 in the following element(s): **voltage driver that produces a compensated voltage**. Claim 1 further recites **wherein the compensated voltage is distributed to form the distributed voltage at the one or more components, and the distributed voltage is degraded relative to the compensated voltage**.

In other words, the output of OA1 would also need to be received at the **one or more components**. This is further reflected by **one or more components, including a feedback component, that receive a distributed voltage** as also recited in claim 1. Hence, for this aspect of the combination rejection to be technically consistent, the output of OA1 must also be received at the other (non-feedback) components.

However, the output of OA1 is not provided external of the standard voltage generator (VLG) in Fig. 27 of Kajigaya et al. Moreover, the rejection in the Office Action sets forth a correspondence between the "one or data receivers (or 'components') (18 and 24 of Fig. 1 of Manning)" as quoted from the first sentence of the last paragraph on page 2 of the Office Action. These differential input buffers 18 and 20 of Manning cannot receive the output of OA1 because this output is not provided external to the standard voltage generator (VLG) of Fig. 27 of Kajigaya et al.

Hence, no combination of Manning and Kajigaya et al. by one of ordinary skill in the art at the time of the invention would have resulted in routing a random internal voltage level (i.e., the output of OA1 from between Q7 and Q55) out of the standard voltage generator (VLG) of Kajigaya et al. and providing this random

internal voltage level to the differential input buffers 18 and 20 of Manning. Thus, it is respectfully submitted that no combination of Manning and Kajigaya et al. can render the claimed invention obvious as represented by claim 1.

Accordingly, no art of record, either alone or in any combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claims:

Claim 1: **one or more components, including a feedback component, that receive a distributed voltage . . . a voltage driver that produces a compensated voltage . . . wherein the compensated voltage is distributed to form the distributed voltage at the one or more components.**

Claim 17: **one or more data receivers that evaluate one or more corresponding data signals relative to a distributed reference voltage . . . a feedback receiver that evaluates the distributed reference voltage relative to a nominal reference voltage to produce a feedback signal . . . a reference voltage driver that produces a compensated reference voltage . . . wherein the compensated reference voltage is distributed to form the distributed reference voltage.**

Claim 43: **receiver means for evaluating a plurality of data signals relative to a distributed reference voltage . . . feedback means for evaluating the distributed reference voltage relative to a nominal reference voltage to produce a feedback signal . . . driver means having a variable gain for producing a compensated reference voltage . . . routing means for routing the compensated reference**

voltage on the integrated circuit to form the distributed reference voltage at the receiver and feedback means.

Claim 53: **a plurality of data receivers that evaluate binary data signals with reference to a distributed reference voltage and that are coupled to the plurality of memory storage cells . . . a feedback receiver that evaluates the distributed reference voltage relative to a nominal reference voltage to produce a feedback signal . . . a reference voltage driver that produces a compensated reference voltage . . . wherein the compensated reference voltage is routed on the memory device to form the distributed reference voltage at the data and feedback receivers.**

Claim 60: **amplifying a nominal voltage by a variable gain to produce a compensated reference voltage . . . routing the compensated reference voltage over approximately impedance-matched resistive conductors to form a distributed voltage . . . evaluating a plurality of signals relative to the distributed voltage . . . evaluating the nominal voltage relative to the distributed voltage.**

Claim 63: **a reference voltage driver that has a variable gain and produces a compensated reference voltage . . . a plurality of receivers having substantially similar input characteristics that evaluate signals relative to a distributed reference voltage, a particular receiver of the plurality of receivers capable of evaluating a nominal reference voltage signal relative to the distributed reference voltage to produce a feedback signal . . .**

wherein the compensated reference voltage is distributed to form the distributed reference voltage.

II. The rejection of at least claims 1, 17, 53, 60, and 63 under 35 U.S.C. 103(a) appears to fail to directly address certain claim elements.

By way of example with respect to claim 1, the Office Action appears to fail to directly address **a nominal voltage**. Consequently, any element(s) of claim 1 that interact and/or interrelate with **a nominal voltage** are likewise not addressed.

It is therefore respectfully submitted that no complete rejection (e.g., no prima facie case under 35 U.S.C. §103(a)) has been instituted against at least claims 1, 17, 53, 60, and 63. Thus, at least claims 1, 17, 53, 60, and 63 are allowable for this additional reason.

CONCLUSION

It is respectfully submitted that all of claims1-73 are allowable, and prompt action to that end is hereby requested.

Respectfully Submitted,

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